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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,076	01/20/2004	Chun-ying Chen	1875.5720000/RES/GSB	7164

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STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/759,076	CHEN ET AL.
	Examiner	Art Unit
	Steven Loke	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5 and 7-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5 and 7-10* is/are rejected.

7)☒ Claim(s) *2 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 2-5 and 7-10 are objected to because of the following informalities: Claim 2, line 9, claim 3, line 2, the phrase "PMOS (P-channel Metal Oxide Semiconductor Field Effect) transistor" is unclear whether it is being referred to "PMOS (P-channel Metal Oxide Semiconductor) field effect transistor". Since there is a second common terminal, it is believed that the terminal (claim 2, line 20) is a first common terminal. Since there is a second common terminal, it is believed that the terminal (claim 4, line 10) is a first common terminal. Claim 5, lines 3, 5, 8, 10, claim 10, lines 3, 5, 8, 10, the word "positive" is unclear whether it is being referred to "positive voltage". Claim 5, lines 7-8, the phrase "PMOS (P-channel Metal Oxide Semiconductor Field Effect) transistors" is unclear whether it is being referred to "PMOS (P-channel Metal Oxide Semiconductor) field effect transistors". Claim 7, line 9, claim 8, line 2, the phrase "NMOS (N-channel Metal Oxide Semiconductor Field Effect) transistor" is unclear whether it is being referred to "NMOS (N-channel Metal Oxide Semiconductor) field effect transistor". Since there is a second common terminal, it is believed that the terminal (claim 7, line 20) is a first common terminal. Since there is a second common terminal, it is believed that the terminal (claim 9, line 10) is a first common terminal. Claim 10, lines 7-8, the phrase "NMOS (N-channel Metal Oxide Semiconductor Field Effect) transistors" is unclear whether it is being referred to "NMOS (N-channel Metal Oxide Semiconductor) field effect transistors". Appropriate correction is required.

2. Claims 7 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses the connection among the first MOS-on-PWELL device, the second MOS-on-PWELL device, the first NMOS transistor and the second NMOS transistor as claimed in claims 7 and 9.

3. Claims 5 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, it is unclear how the first and second plurality of MOS-on-NWELL devices connected to the positive and negative voltages. What terminals in the first and second plurality of MOS-on-NWELL devices are being used to connect to the positive and negative voltages?

In claim 5, it is unclear how the first and second plurality of PMOS transistors connected to the positive and negative voltages. What terminals in the first and second plurality of PMOS transistors are being used to connect to the positive and negative voltages?

In claim 10, it is unclear how the first and second plurality of MOS-on-PWELL devices connected to the positive and negative voltages. What terminals in the first and second plurality of MOS-on-PWELL devices are being used to connect to the positive and negative voltages?

In claim 10, it is unclear how the first and second plurality of NMOS transistors connected to the positive and negative voltages. What terminals in the first and second

plurality of NMOS transistors are being used to connect to the positive and negative voltages?

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: All the claimed subject matters as claimed in claims 5, 8 and 10.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed subject matters of claims 5, 8 and 10 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 8 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Horiguchi et al.

In regards to claim 8, Horiguchi et al. show all the elements of the claimed invention in fig. 34C. It is a capacitor for an integrated circuit, comprising: a first NMOS (N-channel Metal Oxide Semiconductor) field effect transistor (the NMOS formed on the left side of fig. 34C) formed on a substrate [101] and having its source and drain terminals (the terminals that connected to N+ type regions [103]) connected together; a second NMOS transistor (the NMOS formed on the right side of fig. 34C) formed on the substrate [101] and having its source and drain terminals (the terminals that connected to N+ type regions [103]) connected together, wherein a gate [106] of the first NMOS transistor is connected to the source and drain terminals of the second NMOS transistor, and wherein a gate [106] of the second NMOS transistor is connected to the source and drain terminals of the first NMOS transistor.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al.

In regards to claim 3, Horiguchi et al. differ from the claimed invention by not showing a capacitor for an integrated circuit comprising: a first PMOS (P-channel Metal Oxide Semiconductor) field effect transistor formed on a substrate and having its source and drain terminals connected together; a second PMOS transistor formed on the substrate and having its source and drain terminals connected together, wherein a gate of the first PMOS transistor is connected to the source and drain terminals of the second PMOS transistor, and wherein a gate of the second PMOS transistor is connected to the source and drain terminals of the first PMOS transistor.

It would have been obvious for the capacitor for an integrated circuit comprising: a first PMOS (P-channel Metal Oxide Semiconductor) field effect transistor formed on a substrate and having its source and drain terminals connected together; a second PMOS transistor formed on the substrate and having its source and drain terminals connected together, wherein a gate of the first PMOS transistor is connected to the source and drain terminals of the second PMOS transistor, and wherein a gate of the second PMOS transistor is connected to the source and drain terminals of the first PMOS transistor because it is conventional to reverse the conductivity type of all the regions of Horiguchi et al.'s device to form a device complement to that of Horiguchi et al.

10. Claim 2 would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

11. Claim 4 would be allowable if rewritten to overcome the objection set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
August 20, 2005

Steven Loke
Primary Examiner